WHAT IS CLAIMED IS:

1. An image recording apparatus comprising:

a plurality of driven elements which are driven for printing of pixels constructing an image;

a plurality of driving circuits which drive said driven elements;

a memory for storing correction data for controlling the driving of each of said driven elements which is executed by said driving circuits; and

a print controller for temporarily reading out the correction data from said memory and storing prior to a printing operation and transmitting the correction data to said driving circuits after completion of the reading operation of the correction data from said memory.

2. An apparatus according to claim 1, wherein

said memory and said driving circuits are provided in a head, and

said print controller temporarily reads out the correction data from said memory provided in said head and transmits the correction data to the driving circuits provided in the head prior to the printing operation.

3. An apparatus according to claim 1, wherein

compressed correction data is stored in said memory,

said print controller has a decompressing circuit for decompressing the compressed correction data stored in said memory,

and

said print controller reads out the compressed correction data from said memory and decompresses it prior to the printing operation and transmits the decompressed correction data to said driving circuits.

4. An apparatus according to claim 1, wherein said print controller has a compressing circuit for compressing the correction data to be stored into said memory and, when the correction data is stored into said memory, the correction data is compressed by said compressing circuit and written into said memory.

5. An apparatus according to claim 1, wherein said driven elements are LED elements for emitting recording light.

6. An apparatus according to claim 1, wherein

said print controller is constructed so as to be connectable to an external upper apparatus, and

when a read command of the correction data is received from said upper apparatus, said print controller reads out the correction data from said memory and transmits it to said upper apparatus.

7. An apparatus according to claim 1, wherein said driven elements are thermal elements.

8. An image recording apparatus comprising:

a plurality of driven elements which are driven for printing of pixels constructing an image;

a plurality of driving circuits which drive said driven elements and are partitioned into a plurality of driving groups;

a CPU for sending control signals through a plurality of control signal lines to said driving circuits of said driving group corresponding to said signal line so as to make said driving circuits operative every group upon printing operation and sending print data to each of said driving circuits through a print data line;

a memory for storing correction data for correcting the driving of each of said driven elements; and

an auxiliary memory for temporarily storing said correction data from said memory under a control of said CPU so as to supply said correction data of each of said driven elements stored in said memory to said driving mechanisms prior to the printing operation,

wherein said correction data is sent from said auxiliary memory to said driving circuits through said print data lines under a control of said CPU.

9. An apparatus according to claim 8, wherein said memory has control terminals for controlling the operation of said memory and data input/output terminals, and said control terminals and said input/output terminals are connected to said control signal lines, respectively.

10. An apparatus according to claim 9, wherein said memory is subjected to an operation control for writing said correction data into said memory and reading out said correction data into said auxiliary memory by the control signals which are supplied from said control

signal lines to said control terminals connected to said signal lines.

11. An apparatus according to claim 8, wherein said control signal lines are strobe signal lines.

12. An apparatus according to claim 8, wherein said memory is an EEPROM.

13. An apparatus according to claim 8, further comprising compressing circuit for compressing said correction data which is stored in said memory, and wherein said CPU decompresses said compressed correction data read out from said memory and supplies the decompressed data to said driving circuits through said auxiliary memory and said print data lines.

14. An apparatus according to claim 10, wherein

said memory has a data input terminal, a data output terminal, a selection terminal, and a clock terminal, and

each of said control signal lines is connected to each of the terminal.

15. An apparatus according to claim 14, wherein the control signal lines other than the control signal lines which are link-driven are connected to said selection terminal and said clock terminal of said memory.

16. An apparatus according to claim 14, wherein

said memory further has a write inhibition terminal, and

said CPU transmits a permission signal to permit the driving of said driven elements to said driving circuits and said write inhibition terminal of said memory and, when the driving of said driven elements is permitted by said permission signal, the writing operation to said memory is inhibited.